BIASING SCHEME FOR LOW SUPPLY HEADROOM APPLICATIONS

CROSS-REFERENCE TO RELATED APPLICATION(S)

This applications claims the benefit of Provisional Application No. 60/164,988 filed November 11, 1999.

FIELD OF THE INVENTION

The invention relates to analog circuit design, and in particular embodiments to low voltage integrated circuits in which current mirroring is employed.

BACKGROUND OF THE INVENTION

In analog integrated circuitry there is often a requirement to provide a precise ratio of currents based on a reference current. Providing such currents is commonly accomplished using current mirrors.

Modern integrated circuits typically operate with reduced supply voltages, in order to conserve energy and to accommodate low voltage digital circuits. As the components within integrated circuits continue to shrink, circuit breakdown voltages typically decrease and supply voltages decrease accordingly. Because of the lower supply voltages within modern integrated circuits, power supplies used for current mirrors and other analog circuitry may be constrained to operate with reduced supply voltages. Accordingly, the voltage available for the functioning of current mirrors is decreased and performance may suffer. Because of decreasing supply voltages, circuit parameters may have an increasing effect on the current provided by current mirrors. Accordingly, there is a need within the art for improved biasing techniques for use with current mirrors.

SUMMARY OF THE INVENTION

Embodiments of the present invention attempt to maintain the proper current ratio between a reference current and the output current of the current mirrors. Embodiments of the current invention attempt to maintain the proper current ratio between the reference current and output current of current mirrors through methods applied to the reference side of the current mirror. This method of compensation using the reference side of the current mirror may be more effective than attempting to increase the current in the output sides of the current mirror, especially in those cases in which the supply voltage of the output current side is low. If most of the supply voltage is dropped across the load, of the output side of the current mirror, no voltage headroom may be left to perform current regulation necessary to maintain the proper ratio between reference and output currents.

Embodiments of the present invention may include such methods as matching the voltage across the output device in the reference side of the current mirror to the voltage drop in the output device of the output side of the current mirror. Embodiments of the present invention may also include various measures to insure that the internal impedance of the reference side is proportional to the impedance of the output side of the current mirror in such a ratio as to maintain the proper current ration between the reference current and the output current.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the accompanying drawings in which consistent numbers refer to similar parts throughout:

FIG. 1A is a graphical representation of an exemplary environment in which an embodiment of the invention may operate.

FIG. 1B is a circuit diagram of a current mirroring system according to the prior art.

FIG. 2 is a schematic of exemplary prior art multiplying current mirror.

FIG. 3 is a schematic diagram according to an embodiment of the current invention.

FIG. 4 is a schematic diagram of an embodiment of the invention utilizing a multiplying current mirror.

FIG. 4A is a block and schematic diagram of a further embodiment of the invention, in which a voltage supply is added to further improve current mirror matching.

FIG. 5 is a schematic diagram of an implementation of the current mirror illustrated in FIG. 4.

FIG. 6 is a schematic diagram of an embodiment of the invention, illustrating an arrangement of the output devices of a current mirror, which provide current to a differential input circuit.

FIG. 7 is a schematic diagram of an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1A is a graphical representation of an environment in which an embodiment of the invention may operate. In FIG. 1A integrated circuit 101 includes current source 103 which draws a reference current I_{ref}. The current I_{ref} is duplicated by a mirror current source 107, supplying a current of I_{mirror}. The mirror current, I_{mirror}, is supplied to a load 105. Such a configuration as illustrated in FIG. 1A is commonly used within the analog portions of integrated circuits. The current I_{mirror} may be equal to I_{ref}, the reference current, or it may be a multiple of I_{ref}.

FIG. 1B is a circuit diagram of a prior art current mirroring system. The circuit in FIG. 1B attempts to replicate

reference current I_{ref} 125 in the output branch of the circuitry 123. That is, it is desirable to make I_{out} the same value as I_{ref}. In order to make I_{out} equal to I_{ref}, the voltage across the drain source junction (Vds) of device 115 should equal the Vds of device 117. Because devices 115 and 117 are integrated devices, their characteristics are very similar. If the drain voltages of devices 115 and 117 are equal, the currents through the devices will be essentially equal because the gates of the devices are at equal potential, that is, they are tied together. A problem occurs when the common mode voltage at point 123 of the differential input circuit 129 drops. When the voltage at point 123 drops, device 127 (the upper device of the cascode pair 127 and 117) may not remain in saturation. If device 127 comes out of saturation, and goes into triode mode, drain voltage on device 117 will be lower than the drain voltage on device 115. Because the drain voltage on device 117 is lower, the current through device 117 will be lower than the current through device 115 and the output current I_{out} will no longer match the current (or a multiple of the current) produced by the reference source I_{ref} 125. Differential input circuit 129 is shown for the purposes of illustration. In practice, any circuit coupled to the mirror current source I_{out} will experience a similar problem once the voltage at the output of that circuit, i.e., the voltage at point 123 drops sufficiently. The problem is exacerbated in the case where devices 115 and 117 are operated in the degenerative mode, in which resistors are added between the source and ground of devices 115 and 117.

FIG. 2 is a schematic of an example of a prior art multiplying current mirror. FIG. 2 is similar to FIG. 1 except that the current mirroring devices illustrated actually represent multiple devices. That is, for example, the output cascode pair 227 and 217 each represent 20 devices in parallel. Device 215 represents two devices in parallel. Because the ratio of the

number of devices in the reference current source to the number of devices in the output current source is 1 to 10 the output current I_{out} through point 223 will be 10 times the reference current produced by I_{ref} 225. The same type headroom problem can occur whether I_{ref} and I_{out} are equal or multiples. So, for example, if the common mode voltage 223 of the differential input circuit 229, drops low enough (for example, if I_{nn} 219 and I_{np} 221 drop low), the 20 devices in parallel, 227, may begin to come out of saturation and enter triode mode. Once the voltage at 223 drops low enough so that the 20 devices 227 begin to enter triode mode, the voltage at the drains of the 20 devices 217 begins to decrease. Once the voltage at the drains of devices 217 begins to decrease, the drain source voltage across devices 217 follows. When the drain source voltage (Vds) across devices 217 decreases to the point where it is lower than the Vds of devices 215, the current through device 217 will decrease. Accordingly, the current in each device 217 becomes less than the current in each device 215 and the current ratio changes due to the lessening of the output current.

FIG. 3 is a schematic diagram according to an embodiment of the current invention. In FIG. 3, the circuit 329, which is coupled to the output current mirror device 319, is again exemplarily a differential input circuit. Those skilled in the art will realize that the differential input circuit 329 serves as an example of a common load circuit but is not limited to a differential circuit. The present embodiment of the invention is applicable to any type of circuit being driven by a current mirror output device 319.

In FIG. 3 a resistor R309 is added between the source of device 300 and the drain of device 317. Resistor 309 is equal to the impedance of circuit 329, as determined by the parallel combination of resistors 313 and 315.

In the circuitry in FIG. 3, device 319 cannot compensate for the low voltage at its drain because the low voltage is a characteristic of the circuit load. Therefore, to be effective, load compensation will need to be accomplished within device 317, in the reference side of the current mirror.

A voltage is placed on the input of device 300 representing the common mode voltage (that is, it represents the average voltage between input 302 and input 304 of the differential input 329) of the circuit 329. As the voltage at the drain of device 319 changes, so will the voltage at the drain of device 317. Because the Vds of device 317 will track the Vds of device 319, and because the gates of device 317 and 319 are tied together, the reference current will track the output current I_{out}.

FIG. 4 is a schematic diagram of an embodiment of the invention utilizing a multiplying current mirror. In FIG. 4, the output current I_{out} is equal to 10 times the current provided by reference generator 407 thereby providing the desired current ratio of 10 to 1. The input 401 represents a common mode voltage, that is, the average between I_{nn} 402 and I_{np} 404. Since the I_{out} of device 419 represents 20 devices in parallel, and reference device 417 represents two devices in parallel, a 10:1 ratio results. 409 represents the parallel combination of the two resistors 413 and 415. Resistor 409 represents 10 times the resistance of circuit 429 or 20 times each individual resistor 413 or 415. The impedance of the reference side is N times the impedance of the output side of the current mirror (where N is the ratio of the output current to the reference current).

FIG. 4A is a schematic diagram of a further embodiment of the invention, in which a voltage supply is added to further improve current mirror matching. In FIG. 4A a voltage source 423 has been added. In FIG. 4A, just as in FIG. 3, Vds of the reference output device 417 is adjusted to match Vds of the output mirror device 419. The drain voltage of the reference

side device 400, however, is different than the drain voltage of device 403. Voltage source 423 equalizes the voltage on the drain of the current mirror 400 with the drain voltage of devices 403 and 405. By matching the drain voltage of the reference side device 400 with the drain voltage of devices 403 and 405, the voltage between the drain of the driver device 400 and the output device 417 is brought to be more in line with the voltage between the output devices 425 and the drain of device 419.

FIG. 5 is a schematic diagram of an exemplary implementation of a current mirror, similar to that illustrated in FIG. 4. In FIG. 5, the combination of a current source 523, resistance 525 and second current source 527, replaces the voltage supply 423 of FIG. 4A. In FIG. 5, the resistor 525 is calculated such that the current I_{523} times the resistance of 525 equals the voltage supply 423 (as illustrated in FIG. 4A). In addition, current supply 527 is set equal to current supply 523. From Kirchoff's current laws the sum of currents into a node must always equal 0. Thus current I_{525} minus current I_{517} minus current I_{519} minus current I_{527} equals 0. Likewise, current I_{523} plus I_{500} minus I_{525} must equal 0. By setting both equations equal to one another it can be determined that I_{517} plus I_{519} must equal I_{500}. Because devices 517 and 519 are in fact FET-type devices, I_{517} and I_{519} are negligible. Therefore, current I_{500} is also negligible. Thus, the desired voltage drop across resistor 525 can be achieved by considering only the value of the current sources 523 and 527 and the resistance value of resistor 525.

FIG. 6 is a schematic diagram of an alternate embodiment of the invention, illustrating an arrangement of the output devices of a current mirror providing current to a differential input circuit. In FIG. 6, individual output devices 629 and 619 replace a single output device such as device 519 in FIG. 5. In FIG. 6, the differential input circuit 631 has degenerating resistors 613 and 615 coupled together, not in line with the

output current. Such an arrangement can increase the headroom for the output devices of the current mirror. In such an arrangement, however, there could be a larger contribution to thermal noise of differential pair 631 by the current source devices.

FIG. 7 is a schematic diagram of a further embodiment of the invention. In FIG. 7, the circuit 725 which comprises the load for the output side of the current mirror, is replicated in the reference side of the current mirror. Circuit 725 in the reference side of the current mirror is designated as 725_{ref}. Input 721, in addition to being coupled to the gate of device 703, is also coupled to the gate of device 703R. Additionally, the signal 723 which is coupled to the gate of the device 705 is also coupled into the gate of device 705R in the circuit 725_{ref}. In such a manner the circuits 725 and 725_{ref} are made electrically equivalent. By making circuit 725_{ref} and circuit 725 electrically equivalent, the voltage drop across them will be identical. Additionally, the output devices of the reference side of the current mirror and the output side of the current mirror can be degenerated. That is, resistors 713 and 715 may be added to the circuit. In such a way, the current generated in current source 707 is replicated by I_{727} in the output leg of the current mirror.